Code : 041401

B.Tech 4th Semester Exam., 2019

BASIC ELECTRONICS

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

(ii) There are ***NINE*** *questions in this paper.*

(iii) Attempt ***FIVE*** *questions in all.*

(iv) Question No. ***1*** *is compulsory.*

1. Answer the following questions briefly (any *seven*) : 2×7=14

(a) If doping level in a crystal diode is increased, what will happen to the width of depletion layer?

(b) How does Zener diode behave in the breakdown region?

(c) At which voltage avalanche occurs in a diode?

(d) If the maximum DC current rating of diodes in bridge rectifier is 2A, then what is the maximum DC load current?

(e) A half-wave rectifier has an input voltage of 240 V r.m.s. If the the step-down transformer has a turns ratio of 8 : 1, what is the peak load voltage? Ignore diode drop.

(f) If V_{CC} = +20 V, voltage-divider resistor R_1 is 5k Ω and R_2 is 2k Ω, what is the base bias voltage?

(g) When does thermal runaway occur?

(h) With the E-MOSFET, what is the value of drain current when gate input voltage is zero?

(i) What is the bandwidth of an ideal operational amplifier?

(j) If gate current is increased, then what will happen to anode-cathode voltage at which SCR closes?

2. (a) Differentiate between ideal and practical voltage sources. Give their graphical representations and convert 20 V voltage source with its series resistance of 10 Ω into its equivalent current source.

(b) Derive continuity equation for carrier concentration in body of a semiconductor. 7+7=14

3. (a) Derive the expressions for (i) I_{rms}, (ii) I_{dc}, (iii) ripple factor and (iv) efficiency of rectification; in case of full-wave rectifier.

(b) Draw a sketch to show various currents in an *N-P-N* transistor and derive the relationship between various components. 6+8=14

4. (a) A 4 : 1 transformer supplies a bridge rectifier that is driving a load of 400 ohms. If the transformer input is 230 V/50 Hz supply, calculate the d.c. output voltage, *P-I-V* and the output frequency. Assume the rectifier diodes to be ideal.

(b) Draw diode *I-V* characteristics, discuss its temperature dependence and obtain the expression for diode dynamic resistance. 7+7=14

5. (a) Using a common collector *N-P-N* transistor configuration, derive the expressions for voltage gain and current gain.

(b) Design the voltage divider bias circuit to operate from 20 V supply. The bias conditions are $V_{CE} = 5$ V, $V_E = 7$ V and $I_C = 5$ mA. 7+7=14

6. (a) A collector to base circuit has $V_{CB} = 30$ V, $R_B = 200$ kΩ, $R_C = 4$ kΩ and $V_{CE} = 20$ V. Calculate h_{FE} and determine V_{CE}, when a new transistor is replaced having $h_{FE} = 150$.

(b) Draw two-dimensional structure of *n*-channel MOSFET. Explain its working. 7+7=14

7. (a) An *n*-channel FET is utilized by amplifier shown in figure for which $V_P = -3{\cdot}0$ V and $I_{DSS} = 2$ mA. It is desired to bias the circuit at $I_D = 1$ mA,

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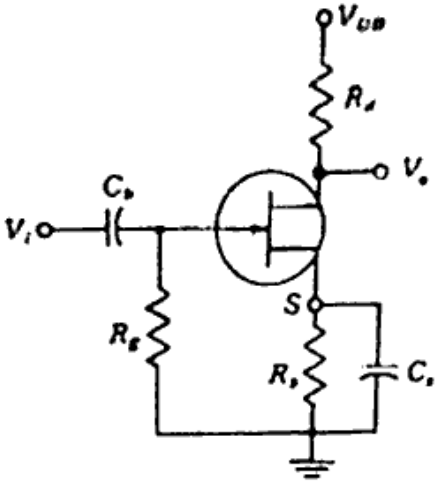
using $V_{DD} = 26$ V. Assume $r_d >> R_d$. Find (i) V_{GS}, (ii) g_m and (iii) R_S.



(b) Explain the working of BJT voltage-divider bias circuit. Derive the expression for Q-point (I_{CQ}, V_{CEQ}) in terms of circuit parameters. 7+7=14

8. (a) Explain a voltage-series feedback amplifier with suitable example.

(b) Using an op-amp, explain the circuits for a voltage gain amplifier (with least components) and current to voltage converter. 7+7=14

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9. *(a)* Explain the working principle of unijunction transistor (UJT).

(b) Describe the structure, symbol and operation of SCR with the help of suitable diagrams. 7+7=14

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