

3. (a) Describe the process of segmentation with diagram.
 (b) What is cache memory? State the importance of cache memory. 7+7
4. (a) Compare between RISC and CISC architecture.
 (b) Explain Flynn's taxonomy on parallel computing. 7+7
5. (a) Write the steps for subtraction of two n-digit unsigned numbers M-N ($N \neq 0$) in base r.
 (b) Subtract 72532-13250 by using the above method. 7+7
6. (a) Explain instruction cycle for pipeline.
 (b) Write the steps, required to process each instruction. 7+7
7. How the instruction cycle in the CPU can be processed with a four segment pipeline? Explain with block diagram. 14
8. (a) Write some application areas where vector processing is used.
 (b) Write the difference between Isolated I/O and Memory mapped I/O. 7+7
9. Short notes : [any 2] 7+7
- (a) Virtual memory
 - (b) Speedup in Pipelining
 - (c) SIMD array processor

Code : 051602

B.Tech 6th Semester Examination, 2017

Computer Architecture

Time : 3 hours

Full Marks : 70

Instructions :

- (i) There are **Nine** Questions in this Paper.
- (ii) Attempt **Five** questions in all.
- (iii) **Question No. 1 is Compulsory.**
- (iv) The marks are indicated in the right-hand margin.

1. **Compulsory Short answers type questions. (Answer any 7)**

2×7=14

- (a) The DMA differs from the interrupt mode by
- (i) The involvement of the processor for the operation
 - (ii) The method accessing the I/O devices
 - (iii) The amount of data transfer possible
 - (iv) Both (i) and (iii)
- (b) When generating physical addresses from logical address the offset is stored in
- (i) Translation look-aside buffer
 - (ii) Relocation register
 - (iii) Page table
 - (iv) Shift register

(c) The computer architecture aimed at reducing the time of execution of instructions is

- (i) CISC
- ☒ (ii) RISC
- (iii) ISA
- (iv) ANNA

(d) In DMA transfers, the required signals and addresses are given by the

- (i) Processor
- (ii) Device drivers
- ☒ (iii) DMA controllers
- (iv) The program itself

(e) Both the CISC and RISC architectures have been developed to reduce the.....

- (i) Cost
- (ii) Time delay
- ☒ (iii) Semantic gap
- (iv) All of the above

(f) In pipelining the task which requires the least time is performed first

- (i) True
- ☒ (ii) False

(g) The DMA controller has registers.

- (i) 4
- (ii) 2
- ☒ (iii) 3
- (iv) 1

(h) In memory-mapped I/O.....

- ☒ (i) The I/O devices and the memory share the same address space.
- (ii) The I/O devices have a separate address space
- (iii) The memory and I/O devices have an associated address space
- (iv) A part of the memory is specifically set aside for the I/O operation

(i) Any condition that causes a processor to stall is called as

- ☒ (i) Hazard
- (ii) Page fault
- (iii) System error
- (iv) None of the above

(j) The situation where in the data of operands are not available is called _____

- ☒ (i) Data hazard
- (ii) Stock
- (iii) Deadlock
- (iv) Structural hazard

417 2. (a) What is DMA? Explain the working principle of DMA using block diagram.

(b) What is Interrupt cycle? Explain with block diagram and flow chart.

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