Code : 051602

B.Tech 6th Semester Exam., 2015

COMPUTER ARCHITECTURE

Time : 3 hours *Full Marks* : 70

Instructions :

(i) All questions carry equal marks.

(ii) There are ***NINE*** *questions in this paper.*

(iii) Attempt ***FIVE*** *questions in all.*

(iv) Question No. ***1*** *is compulsory.*

1. Choose the correct option (any *seven*) :

(a) The special memory used to store micro-instructions of a computer is

(i) control table

(ii) control memory

(iii) control unit

(iv) control space

(b) In zero-address instruction method, the operands are stored in

(i) registers

(ii) accumulators

(iii) stack

(iv) cache

(c) The disadvantage of the hardwired approach is that
  (i) it is less flexible
  (ii) it cannot be used for complex instructions
  (iii) it is costly
  (iv) Both (i) and (iii)

(d) The number of successful accesses to memory stated as fraction is called as
  (i) hit rate
  (ii) miss rate
  (iii) success rate
  (iv) access rate

(e) The addressing mode, where you directly specify the operand value is
  (i) immediate
  (ii) direct
  (iii) definite
  (iv) relative

(f) To increase the speed of memory access in pipelining, we make use of
  (i) special memory locations
  (ii) special purpose registers
  (iii) cache
  (iv) buffers

(g) The associatively mapped virtual memory makes use of
  (i) TLB
  (ii) page table
  (iii) frame table
  (iv) None of the above

(h) —— are used to interface between stages of synchronous pipeline.
  (i) Locks
  (ii) Latches
  (iii) Interface control
  (iv) None of the above

(i) —— refers to the maximum data transfer rate.
  (i) MIPS
  (ii) CPI
  (iii) Bandwidth
  (iv) None of the above

(j) —— refers to the worst case time delay for a unit message to be transferred through the network.
  (i) Latency
  (ii) Bandwidth
  (iii) Worst-fit
  (iv) None of the above

2. (a) What is microprogrammed control unit? Explain the difference between hardwired control and microprogrammed control.

(b) Describe the organization and working of microprogrammed control.

3. (a) Explain direct and indirect addressing schemes.

(b) Compare CISC and RISC architecture.

4. (a) What are the functions of input/output interface?

(b) What is DMA? Explain step-by-step working of DMA controller.

5. (a) Assume a computer having 64-word RAM (1 word = 16 bits) and cache memory of 8 blocks (block size = 32 bits). Where can we find main memory location 25 in cache if *(i)* associative mapping, *(ii)* direct mapping and *(iii)* two-way set associative mapping are used?

(b) How can the cache memory and interleaved memory mechanisms be used to improve the overall processing speed of a computer system?

(Continued)

6. (a) How can parallelism be realized in uniprocessor system?

(b) What is the basis for structural classification of parallel computers? Explain UMA, NUMA and COMA models.

7. (a) What is pipelining? How can it be implemented in a processor?

(b) What are the performance matrices for pipelining? Discuss the issues in pipelining.

8. (a) Draw the diagram and show the organization of SIMD array processor.

(b) Define the following terms :

(i) Broadcast and multicast networks

(ii) Mesh versus Torus

(iii) Crossbar network

9. (a) Show that step-by-step multiplication process using Booth's algorithm when (–13) is multiplied by (+15).

(b) Evaluate the arithmetic statement

$$X = A - B + C * (D - E)$$

using general registers with two address instructions and three address instructions.

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