Code : 041771

B.Tech 7th Semester Exam., 2017

VLSI DESIGN

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

(ii) There are ***NINE*** *questions in this paper.*

(iii) Attempt ***FIVE*** *questions in all.*

(iv) Question No. ***1*** *is compulsory.*

1. Answer any *seven* questions : 2×7=14

(a) Draw the *I-V* characteristic of MOS transistor.

(b) What is the advantage of using a pseudo-N-MOS logic over the CMOS logic?

(c) What are the factors that cause timing failures in logic circuits?

(d) Write a note on transport delay.

(e) What is the objective of layout design rules?

(f) What are the factors that cause static power dissipation in CMOS circuit?

(g) What are the stages at which a chip can be tested?

(h) Compare between CMOS and BiCMOS technology.

(i) Define power dissipation in CMOS logic circuit.

(j) What is subprogram overloading?

2. *(a)* What do you mean by channel length modulation in MOS transistors? How can you use MOS transistors as a switch? 8

(b) An nMOS transistor has the following parameters :

Gate oxide thickness = 10 nm
Relative permittivity of gate oxide = 3·9
Electron mobility = 520 cm^2/V-sec
Threshold voltage = 0·7 V
Permittivity of free space = $8 \cdot 85 \times 10^{-14}$ F/cm
and W/L = 8

Calculate the drain current when $V_{GS} = 2\,V$, $V_{DS} = 1 \cdot 2\,V$ and $V_{GS} = 2\,V$, $V_{DS} = 2\,V$, and also compute the gate oxide capacitance per unit area. Note that W and L refer to the width and length of the channel respectively. 6

3. Explain, in detail with neat diagram, the process steps involved in fabrication of the *n*-channel MOSFET. 14

4. *(a)* Discuss, in detail with neat layout, the design rules for the CMOS inverter. 8

(b) What is the importance of delay models? Define gate delay. Which parameters determine the gate delay? 6

5. *(a)* Design the function $Y = (A + B + C) \cdot D$ using CMOS compound gate. Draw the stick diagram of this function. 7

(b) Discuss the dynamic and static power dissipation in CMOS logic circuits. 7

6. *(a)* Why do we need a CAD tool for VLSI design? 3

(b) What do you mean by RTL synthesis, placement and routing? 7

(c) Explain floor planning. 4

7. *(a)* Explain the principle of SOI technology with neat diagrams. Discuss its advantages and disadvantages. 8

(b) Compare the architecture of CPLD and FPGA. 6

8. *(a)* Draw and explain the logic diagram and configuration of Xilinx SRAM cell. 8

(b) Explain the CMOS logic design strategy with the help of the terms hierarchy, regularity and locality. 6

9. Write short notes on the following : 7×2=14

(a) Latch up

(b) Twin-tub process

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