Code : 041561

B.Tech 5th Semester Exam., 2018

MICROELECTRONICS : IC DESIGN AND FABRICATION

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

*(ii) There are **NINE** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

*(iv) Question No. **1** is compulsory.*

1. Choose the correct answer/Fill in the blanks (any *seven*) : 2×7=14

(a) Photoresist layer is formed using

(i) high-sensitive polymer

(ii) light-sensitive polymer

(iii) polysilicon

(iv) silicon dioxide

(b) In NMOS device, gate material could be

(i) silicon

(ii) polysilicon

(iii) boron

(iv) phosphorous

(c) In NMOS fabrication, etching is done using

(i) plasma

(ii) hydrochloric acid

(iii) sulphuric acid

(iv) sodium chloride

(d) Which capacitance must be higher?

(i) Metal to polysilicon capacitance

(ii) Metal to substrate capacitance

(iii) Metal to metal capacitance

(iv) Diffusion capacitance

(e) In CMOS manufacturing process sheet resistance is used instead of resistivity because

(i) resistivity is same for all doped regions

(ii) resistivity and thickness are characteristics which cannot be controlled by the circuit designer and it is expressed as the single sheet resistance parameter

(iii) sheet resistance is dimensionless quantity

(iv) sheet resistance is equal to resistivity

(f) What is 'lithography' used for, in semiconductor manufacturing?

(i) To dope semiconductors

(ii) To deposit amorphous films on semiconductors

(iii) To deposit polycrystalline films on semiconductors

(iv) To grow crystalline films on semiconductors

(v) To produce patterns in the films deposited on semiconductors

(g) The maximum operating frequency is scaled by

(i) $1/\alpha^2$

(ii) β/α^2

(iii) α^2/β

(iv) 1

(h) The diffusion and polysilicon layers are connected together using

(i) butting contact

(ii) buried contact

(iii) separate contact

(iv) Cannot be connected

(i) The deposition of metal or silicon alloy can be done by

(i) sputtering

(ii) evaporation

(iii) sputtering and evaporation

(iv) Deposition should not be made

(j) Contact cuts should be ____ apart.

(i) 2λ

(ii) 3λ

(iii) 4λ

(iv) λ

2. (a) Describe the Bi-CMOS process flow. Make a comparison table between CMOS and bipolar technology on the basis of static power dissipation, input impedance, noise margin, packing density, delay sensitivity to load, output drive current, trans-conductance and directional capability. 7

(b) Draw the stick diagram and layout for NMOS shift register cell. 7

3. (a) Explain the need of a design rule for layout generation. Explain the lambda-based design rule for layout. 7

(b) Define sheet resistance. The Fermi level of an *n*-type germanium film is 0·2 eV above the intrinsic Fermi level towards the conduction band. The thickness of the film is 0·5 μm. Calculate the sheet resistance of the film. Given :

$n_i = 10^{13}\,cm^{-3}$, $\mu_n = 3500 cm^2/V-s$

$\mu_p = 1500 cm^2/V-s$, $kT/q = 26\,mV$ 7

4. (a) Find out the delay of a CMOS inverter pair. 7

(b) What is the need of scaling? How does scaling affects the sub-threshold current? Also, explain the effect of scaling on maximum electric field across depletion layer in a MOSFET and its breakdown voltage (BV). 7

5. (a) Why does zone processes grow material with higher purity compared to the Czrolaski or Gradient freeze technique? Explain the zone refining and zone levelling. 7

(b) Derive the diffusion equation. Using the diffusion equation, explain the diffusion process due to unlimited source if rate of diffusion is constant. 7

6. (a) Explain the process of oxide (SiO_2) formation in Si showing the chemical reactions due to (i) dry oxygen and (ii) water vapour. 7

(b) Explain the chemical vapour deposition (CVD) process with neat diagram. 7

7. (a) What are the different resolution enhancement techniques? Explain the phase shift principle using a phase shifting mask (PSM). What is the phase conflict problem in PSM? 7

(b) Why is transmission gate better compared to the pass transistor logic? Implement the following logic using transmission gate logic. Also, draw its stick diagram :

$$f(A, B) = \overline{A}B + A\overline{B}$$ 7

8. (a) Explain the reactive-ion etching (RIE) with a neat diagram showing the different steps. Why is it difficult to etch Al-Cu alloy with high Cu content? 7

(b) Explain in brief (i) isolation using *p-n* junction and (ii) mesa isolation. 7

9. (a) Why is CMOS ratio-less logic whereas NMOS is a ratioed logic? Determine the pull-up to pull-down ratio for an NMOS inverter driven by another NMOS inverter. 7

(b) Draw the schematic diagrams and explain the working principle of three-transistor dynamic RAM cell. 7

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